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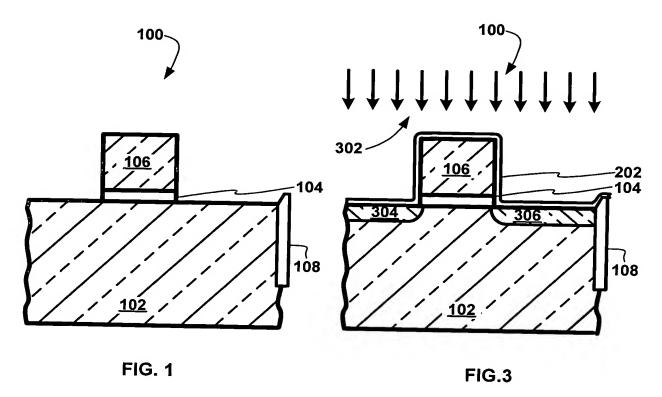
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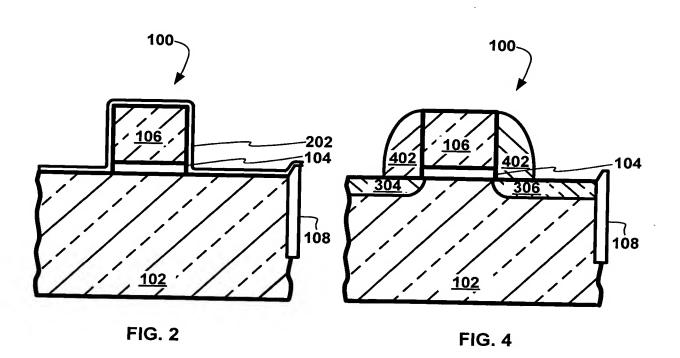
Inventors: Darin A. Chan, et al.

Docket No.: H1844

Contact: Mikio Ishimaru (408) 738-0592

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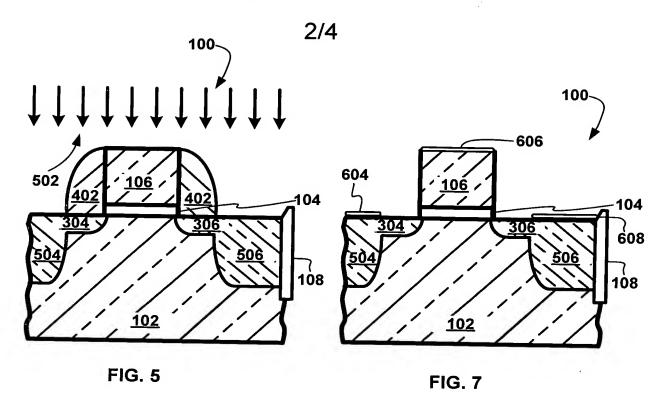
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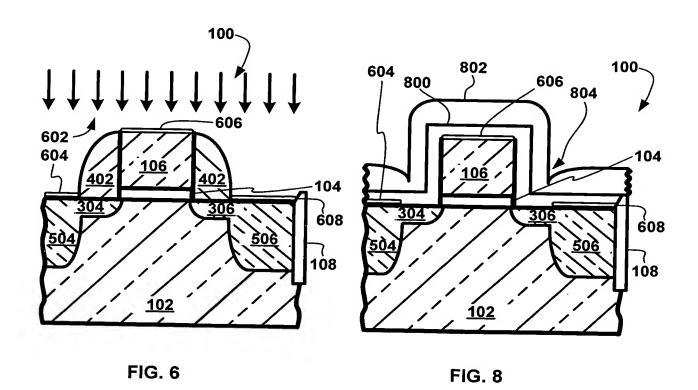
TECHNOLOGY

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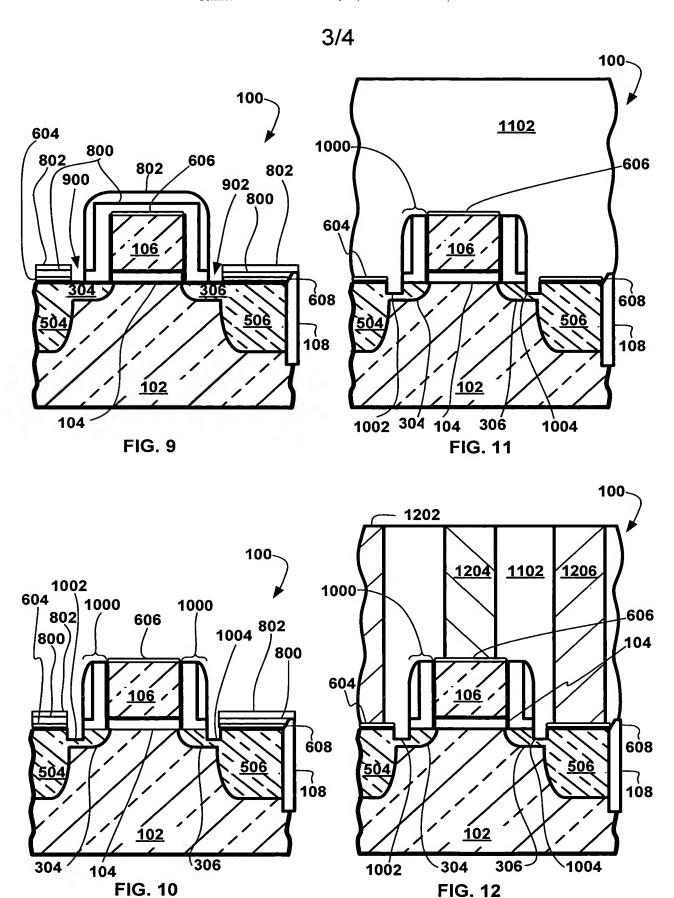
Title: TRENCHES TO REDUCE LATERAL SILICIDE

GROWTH IN INTEGRATED CIRCUIT

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Docket No.: H1844 Contact: Mikio Ishimaru (408) 738-0592 4/4 1300 PROVIDING A SEMICONDUCTOR SUBSTRATE 1302 FORMING A GATE DIELECTRIC ON THE SEMICONDUCTOR SUBSTRATE <u>1304</u> FORMING A GATE ON THE GATE DIELECTRIC <u>1306</u> FORMING SOURCE/DRAIN JUNCTIONS IN THE SEMICONDUCTOR SUBSTRATE <u>1308</u> FORMING A SILICIDE ON THE SOURCE/DRAIN JUNCTIONS AND ON THE GATE 1310 FORMING TRENCHES IN THE SEMICONDUCTOR SUBSTRATE AROUND THE GATE <u>1312</u> DEPOSITING AN INTERLAYER DIELECTRIC ABOVE THE SEMICONDUCTOR SUBSTRATE <u>1314</u> FORMING CONTACTS IN THE INTERLAYER DIELECTRIC TO THE

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TECHNOLOGY
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FIG. 13

SILICIDE 1316